PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P 02 005 WO	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/GB 03/01441	International filing date *(day/month/year)* 02.04.2003	Priority date *(day/month/year)* 02.04.2003
International Patent Classification (IPC) or both national classification and IPC H03L7/07		
Applicant TRAVIS, Christopher Julian		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 14 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☒ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
02.11.2004	29.07.2005
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Kahn, K-D Telephone No. +49 89 2399-2253

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB 03/01441

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1-74 as originally filed

Claims, Numbers

1-90 received on 04.06.2005 with letter of 01.06.2005

Drawings, Sheets

1/18-18/18 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

IV. Lack of unity of invention

1. In response to the invitation to restrict or pay additional fees, the applicant has:

   ☐ restricted the claims.

   ☒ paid additional fees.

   ☐ paid additional fees under protest.

   ☐ neither restricted nor paid additional fees.

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose, according to Rule 68.1, not to invite the applicant to restrict or pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rules 13.1, 13.2 and 13.3 is

   ☐ complied with.

   ☒ not complied with for the following reasons:

   see separate sheet

4. Consequently, the following parts of the international application were the subject of international preliminary examination in establishing this report:

   ☐ all parts.

   ☒ the parts relating to claims Nos. 1 - 22 .

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	2 - 22
	No:	Claims	1
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1 - 22
Industrial applicability (IA)	Yes:	Claims	1 - 22
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item IV
Lack of unity of invention

This Authority considers that there are 3 inventions covered by the claims indicated as follows:
Subject 1 claims a hybrid numeric-analog clock synchroniser for establishing a clock or carrier frequency locked to a timing reference.
Subject 2 claims a high performance number-controlled oscillator for use as a NCO in the hybrid numeric-analog clock synchroniser defined in subject 1.
Subject 3 claims a combined clock- and frame asynchrony detector for use as the second detector for the cascade form of the hybrid numeric-analog clock synchroniser defined in subject 1.
The above subjects 1 (the hybrid numeric-analog clock synchroniser), 2 (the high performance number-controlled oscillator) and 3 (the combined clock- and frame asynchrony detector) share neither the same nor any corresponding special technical features as required by Rule 13.2 PCT, second sentence.

The Applicants have been invited by the International Searching Authority to pay additional fees to have the search results on the above-mentioned different inventions included in the international search report ISR. The Applicants have paid additional fees for the different subjects as defined by the Searching Authority. Therefore the International Search Report covers all claims.

According their letter dated 02.11.2004 accompanying the demand under Article 31 of the PCT, the applicants have requested a detailed international preliminary examination only for the first invention identified in the ISR, namely claims 1 to 22.

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following document/s/:
   D1: WO 99/33182 A (KONINKL PHILIPS ELECTRONICS NV ;PHILIPS SVENSKA AB (SE)) 1 July 1999,
   D2: US-A-5 790 614 (POWELL WILLIAM E) 4 August 1998,
   D3: EP-A-1 104 111 (LUCENT TECHNOLOGIES INC) 30 May 2001,
   D4: EP-A-0 698 968 (DEUTSCHE TELEPHONWERK KABEL) 28 February 1996
   D5: WO 00/18008 A (FRIEDRICH DIRK ;ROZMANN MICHAEL (DE); SIEMENS AG (DE)) 30 March 2000.

2. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 1 is not new in the sense of Article 33(2) PCT.

2.1 The document D1 discloses in the passages cited in the ISR (the references in parentheses applying to this document):
- a method of establishing an output clock signal (output of VCO 103) on the basis of an input timing reference (incoming clock, page 5, line 26),

said method comprising the steps of
- attenuating jitter of said input timing reference to produce a control signal (incoming frequency value, page 6, line 9),
- providing an intermediate clock signal (output signal, page 6, line 13) on the basis of said control signal (incoming frequency value, page 6, line 9),
- the intermediate clock signal being justified to a local clock (Sysclock) and being spectrum controlled (page 6, lines 13 - 16), and
- providing said output clock signal (output of VCO 103) on the basis of said intermediate clock signal (output signal, page 6, line 13) by attenuating jitter of said intermediate clock signal (page 6, lines 17 - 20).

Claim 1 furthermore requires that
- said output clock signal comprises an output event clock component and an output framing component.

However, although not mentioned explicitly in D1, it is common practice in the field of phase locked loop circuits applied in optical disc read or write devices to generate all necessary clock signals required by the devices in the PLL, and especially read/write clocks and framing clocks. Such feature therefore is considered implicitly disclosed in D1.

Therefore the claim is not allowable due to a lack of novelty.

In addition, it is noted that the feature that the output clock comprises "an output framing component" is not related to and does not achieve any functional interaction with the remaining features defined in the claim. The said feature therefore merely constitutes a non-inventive **aggregation** of features.

3. Dependent claims 2 - 22 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step, see documents D1 - D5 and the corresponding passages cited in the search report.

Patent Claims

1. Method of establishing an output clock signal (OC) on the basis of an input timing reference (TR), said method comprising the steps of

attenuating jitter of said input timing reference (TR) to produce a control signal (103),

providing at least one intermediate clock signal (IC) on the basis of said control signal (103), at least one of said intermediate clock signals (IC) being justified to a local clock (LC) and being spectrum controlled, and

providing said output clock signal (OC) on the basis of said at least one intermediate clock signal (IC) by attenuating jitter of said at least one intermediate clock signal (IC), said output clock signal (OC) comprising an output event clock component (OEC) and an output framing component (OFS).

2. Method of establishing an output clock signal (OC) according to claim 1, whereby at least a part of the jitter of said at least one intermediate clock signal (IC) comprises justification jitter (JJ) originating from said justification to said local clock (LC).

3. Method of establishing an output clock signal (OC) according to claim 1 or 2, whereby said justification and spectrum control is performed numerically.

4. Method of establishing an output clock signal (OC) according to any of the claims 1-3, whereby said attenuation of jitter of said input timing reference (TR) is performed by using low-pass filtering.

5. Method of establishing an output clock signal (OC) according to any of the claims 1-4, whereby said justification is performed by means of a number-controlled oscillator (NCO).

6. Method of establishing an output clock signal (OC) according to any of the claims 1-5, whereby a control input of said number-controlled oscillator (NCO) comprises a period control input.

7. Method of establishing an output clock signal (OC) according to any of the claims 1-6, whereby said spectrum control comprises dithering.

8. Method of establishing an output clock signal (OC) according to any of the claims 1-7, whereby said spectrum control comprises noise shaping.

9. Method of establishing an output clock signal (OC) according to any of the claims 1-8, whereby said local clock (LC) is derived from or comprises a stable reference clock (SC).

10. Method of establishing an output clock signal (OC) according to any of the claims 1-9, whereby said stable reference clock (SC) comprises a crystal oscillator.

11. Method of establishing an output clock signal (OC) according to any of the claims 1-10, whereby said local clock (LC) is derived from said output clock signal (OC).

12. Method of establishing an output clock signal (OC) according to any of the claims 1-11, whereby said attenuation of jitter of said input timing reference (TR) is performed by means of a first block (FBLK), which preferably comprises a time-locked loop, with reference to a stable reference clock (SC).

13. Method of establishing an output clock signal (OC) according to any of the claims 1-12, whereby at least a part of said justification jitter (JJ) is biased into a higher frequency band.

14. Method of establishing an output clock signal (OC) according to any of the claims 1-13, whereby said justification jitter (JJ) is low-pass filtered by means of a second block (SBLK), which preferably comprises a phase-locked loop.

15. Method of establishing an output clock signal (OC) according to any of the claims 1-14, whereby said second block (SBLK) produces a multiplied clock (OEC).

16. Method of establishing an output clock signal (OC) according to any of the claims 1-15, whereby said second block (SBLK) further produces a frame signal (OFS), said frame signal (OFS) being established by means of frequency division of said multiplied clock (OEC).

17. Method of establishing an output clock signal (OC) according to any of the claims 1-16, whereby each of said intermediate clock signals (IC) is established by means of at least one numeric stage (FBLK).

18. Method of establishing an output clock signal (OC) according to any of the claims 1-17, whereby said attenuating jitter of said at least one intermediate clock signal (IC) is performed by means of at least one analog stage (SBLK).

19. Method of establishing an output clock signal (OC) according to any of the claims 1-18, whereby said at least one analog stage (SBLK) is adapted for attenuating jitter partly or mainly originating from said at least one numeric stage (FBLK).

20. Method of establishing an output clock signal (OC) according to any of the claims 1-19, whereby each of said intermediate clock signals (IC) is justified to a corresponding local clock (LC) and justification jitter associated with said justification to said local clock is spectrum controlled.

21. Method of establishing an output clock signal (OC) according to any of the claims 1-20, whereby at least one of said intermediate clock signals (IC) comprises

an intermediate event clock component (IEC) and an intermediate framing component (IFS), said intermediate framing being established on the basis of said intermediate event clock by means of frequency division.

22. Method of establishing an output clock signal (OC) according to any of the claims 1-21, whereby said output clock signal (OC) comprises an output event clock component (OEC) and an output framing component (OFS), said output framing being established on the basis of said output event clock by means of frequency division.

23. Method of establishing an event clock (EC) comprising a stream of event-clock pulses (ECP1..ECPn)

on the basis of a master clock (MC) and on the basis of a stream of period control representations (PCR1..PCRn),

the values of said period control representations (PCR1..PCRn) representing the desired period of the event clock (EC) with respect to that of the master clock (MC),

whereby each of said event-clock pulses (ECP1..ECPn) is established on the basis of an associated master-clock pointer (MCP),

in which said master-clock pointers (MCP) form a stream of master-clock pointers (MCP), which stream is derived from said stream of period control representations (PCR1..PCRn) by a process which comprises accumulation and resolution reduction and where an error signal associated with said resolution reduction is spectrum controlled.

24. Method of establishing an event clock (EC) according to claim 23, whereby said accumulation precedes said resolution reduction.

25. Method of establishing an event clock (EC) according to claim 23 or 24, whereby said resolution reduction precedes said accumulation.

26. Method of establishing an event clock (EC) according to any of the claims 23-25, whereby said resolution reduction may comprise wordlength reduction, quantization, truncation or rounding.

27. Method of establishing an event clock (EC) according to any of the claims 23-26, whereby said event-clock pulses (ECP1..ECPn) are justified to edges of said master clock (MC).

28. Method of establishing an event clock (EC) according to any of the claims 23-27, comprising the steps of

establishing a representation of an idealized clock comprising a stream of target times (TT) on the basis of period control representations (PCR1..PCRn),

justifying said idealized clock to said master clock (MC) while performing spectrum control of the associated justification jitter,

thereby facilitating number-controlled oscillation with improved control of said justification jitter.

29. Method of establishing an event clock (EC) according to any of the claims 23-28, whereby said period control representations (PCR1..PCRn) are digital.

30. Method of establishing an event clock (EC) according to any of the claims 23-29, whereby said period control representations (PCR1..PCRn) are analog.

31. Method of establishing an event clock (EC) according to any of the claims 23-30, whereby said period control representations (PCR1..PCRn) are consecutive components of a discrete-time period control representation signal (PCR).

32. Method of establishing an event clock (EC) according to any of the claims 23-31, whereby said master-clock pointers (MCP) are established on the basis of multiple previous period control representations (PCR1..PCRn).

33. Method of establishing an event clock (EC) according to any of the claims 23-32, whereby said master-clock pointers (MCP) are established on the basis of multiple previous period control representations (PCR1..PCRn) thereby facilitating a continuous accurate establishment of event-clock pulses (ECP1..ECPn).

34. Method of establishing an event clock (EC) according to any of the claims 23-33, whereby said master-clock pointers (MCP) are established on the basis of at least two previous period control representations (PCR1..PCRn) thereby facilitating accurate control of the mean period between consecutive event-clock pulses (ECP1..ECPn).

35. Method of establishing an event clock (EC) according to any of the claims 23-34, whereby said master-clock pointers (MCP) are established on the basis of all previous period control representations (PCR1..PCRn).

36. Method of establishing an event clock (EC) according to any of the claims 23-35, whereby said master-clock pointers (MCP) are established on the basis of integrated period control representations (PCR1..PCRn).

37. Method of establishing an event clock (EC) according to any of the claims 23-36, whereby said master clock (MC) comprises a single-wire clock.

38. Method of establishing an event clock (EC) according to any of the claims 23-37, whereby said master clock (MC) comprises a multiphase clock.

39. Method of establishing an event clock (EC) according to any of the claims 23-38, whereby said master clock (MC) comprises a sequence of master-clock edges.

40. Method of establishing an event clock (EC) according to any of the claims 23-39, whereby a master-clock edge addresser (CR) is synchronized with said master clock (MC), thereby facilitating the selection of those of said master-clock edges that are pointed to by said master-clock pointers (MCP).

41. Method of establishing an event clock (EC) according to any of the claims 23-40, whereby said master-clock edge addresser (CR) comprises a counter (CNT) and a comparator (COM).

42. Method of establishing an event clock (EC) according to any of the claims 23-41, whereby said master-clock edge addresser (CR) comprises a multiplexer (MPX).

43. Method of establishing an event clock (EC) according to any of the claims 23-42, whereby said master-clock edge addresser (CR) comprises a differentiator and a multi-modulus divider.

44. Method of establishing an event clock (EC) according to any of the claims 23-43, whereby said period control representations (PCR1..PCRn) are established on the basis of a period control input (PC).

45. Method of establishing an event clock (EC) according to any of the claims 23-44, whereby said period control input (PC) comprises a continuous-time signal.

46. Method of establishing an event clock (EC) according to any of the claims 23-45, whereby said period control input (PC) comprises an analog signal.

47. Method of establishing an event clock (EC) according to any of the claims 23-46, whereby said period control representations (PCR1..PCRn) comprise numeric representations of said period control input (PC).

48. Method of establishing an event clock (EC) according to any of the claims 23-47, whereby said period control representations (PCR1..PCRn) comprise said period control input (PC).

49. Method of establishing an event clock (EC) according to any of the claims 23-48, whereby the process of establishing said master-clock pointers (MCP) comprises quantization.

50. Method of establishing an event clock (EC) according to any of the claims 23-49, whereby the quantization error is subject to spectrum control.

51. Method of establishing an event clock (EC) according to any of the claims 23-50, whereby said spectrum control comprises dithering.

52. Method of establishing an event clock (EC) according to any of the claims 23-51, whereby said spectrum control comprises noise shaping.

53. Method of establishing an event clock (EC) according to any of the claims 23-52, whereby said spectrum control comprises dithering and noise shaping.

54. Method of establishing an event clock (EC) according to any of the claims 23-53, whereby the resolution of said period control representations (PCR1..PCRn) is greater than the resolution of said master-clock pointers (MCP).

55. Clock synchronizer for establishment of an output clock signal (OC) according to any of the claims 1-22 or any of the claims 86-90.

56. Clock synchronizer for establishment of an output clock signal (OC) according to claim 55, further comprising a number-controlled oscillator (NCO) according to any of the claims 23-54.

57. Clock synchronizer for establishment of an output clock signal (OC) according to claim 55 or 56, further comprising a circuit for attenuating jitter of an input timing reference (TR), said circuit comprising a number-controlled oscillator (NCO) adapted for establishment of an intermediate clock signal (IC) on the basis of said input timing reference (TR).

58. Clock synchronizer for establishment of an output clock signal (OC) according to any of the claims 55-57, further comprising jitter filtering means (SBLK) adapted for providing said output clock signal (OC) on the basis of said intermediate clock signal (IC).

59. Number-controlled oscillator (NCO) comprising means for establishment of an event clock (EC) according to any of the claims 23-54.

60. Method of establishing at least one output signal (CDO) on the basis of at least two input signals (IS1, IS2),
where said input signals each comprise at least
a first component (IS1A, IS2A) and
a second component (IS1B, IS2B) and

where said output signal (CDO) is established fully or partly on the basis of the asynchrony of said first components (IS1A, IS2A) of at least two of said input signals (IS1, IS2) when at least one first predefined criterion is fulfilled and

where said output signal (CDO) is established fully or partly on the basis of the asynchrony of said second components (IS1B, IS2B) of at least two of said input signals (IS1, IS2) when at least one second predefined criterion is fulfilled.

61. Method of establishing at least one output signal (CDO) according to claim 60, whereby said at least one output signal (CDO) represents the phase angle between said at least two of said input signals.

62. Method of establishing at least one output signal (CDO) according to claim 60 or 61, whereby said at least one output signal (CDO) represents the time interval between said at least two of said input signals.

63. Method of establishing at least one output signal (CDO) according to any of the claims 60-62, whereby said input signals (IS1, IS2) are mutually asynchronous.

64. Method of establishing at least one output signal (CDO) according to any of the claims 60-63, whereby said first components (IS1A, IS2A) of said input signals (IS1, IS2) comprise event-clock-representative components.

65. Method of establishing at least one output signal (CDO) according to any of the claims 60-64, whereby said second components (IS1B, IS2B) of said input signals (IS1, IS2) comprise frame-sync-representative components.

66. Method of establishing at least one output signal (CDO) according to any of the claims 60-65, whereby at least one of said input signals (IS1, IS2) comprises feedback signals of a phase-locked loop.

67. Method of establishing at least one output signal (CDO) according to any of the claims 60-66, whereby at least one of said input signals (IS1, IS2) comprises feedback signals of a time-locked loop.

68. Method of establishing at least one output signal (CDO) according to any of the claims 60-67, whereby said first and second components of at least one of said input signals (IS1, IS2) are inherent in a multiphase representation of that signal.

69. Method of establishing at least one output signal (CDO) according to any of the claims 60-68, whereby said first and second components of at least one of said input signals (IS1, IS2) comprise two separately wired signals.

70. Method of establishing at least one output signal (CDO) according to any of the claims 60-69, whereby said first and second components of at least one of said input signals (IS1, IS2) are comprised in a composite signal.

71. Method of establishing at least one output signal (CDO) according to any of the claims 60-70, whereby said first predefined criterion comprises said asynchrony of said second components (IS1B, IS2B) substantially being smaller than the period of one of said first components (IS1A, IS2A).

72. Method of establishing at least one output signal (CDO) according to any of the claims 60-71, whereby said second predefined criterion comprises said asynchrony of said second components (IS1B, IS2B) substantially exceeding the period of one of said first components (IS1A, IS2A).

73. Method of establishing at least one output signal (CDO) according to any of the claims 60-72, whereby at least one of said predefined criteria is established on the basis of the reliability of at least one of said components (IS1A, IS1B, IS2A, IS2B).

74. Method of establishing at least one output signal (CDO) according to any of the claims 60-73, whereby at least one of said predefined criteria is established on the basis of a quality measure that relates to the performance of a system applying said method.

75. Method of establishing at least one output signal (CDO) according to any of the claims 60-74, whereby said second component (IS1B, IS2B) groups an integer

number of clock events of said first components (IS1A, IS2A) into frames and where said number is greater than two.

76. Asynchrony detector (CD) comprising means for establishing at least one output signal (CDO) according to any of the claims 60-75.

77. Asynchrony detector (CD) according to claim 76, further comprising filtering means (SLF) for filtering said output signal (CDO).

78. Asynchrony detector (CD) according to claim 76 or 77, wherein said output signal (CDO) is used as control signal for an oscillator (VCO).

79. Asynchrony detector (CD) according to any of the claims 76-78, wherein said asynchrony detector forms part of a phase-locked loop.

80. Asynchrony detector (CD) according to any of the claims 76-79, wherein said asynchrony detector forms part of a time-locked loop.

81. Asynchrony detector (CD) according to any of the claims 76-80, wherein said output signal (CDO) is established by means of

at least two synchronous state machines (RSSM, FSSM), each acting on one of said input signals (IS1, IS2) and on at least one signal from at least one other of said synchronous state machines (RSSM, FSSM),

at least one frame offset counter (FOC),

at least one combinatorial block (CMB) adapted to process event count values derived from said synchronous state machines (RSSM, FSSM) and to process force signals (FUP, FDN) derived from said frame offset counter (FOC).

82. Asynchrony detector (CD) according to any of the claims 76-81, wherein said output signal (CDO) is established by means of a set of at least two basic asynchrony

detectors (DET1, DET2, DET3, DETn), said set of detectors being adapted to act on multiphase clocks (MPIC, MPFC).

83. Asynchrony detector (CD) according to any of the claims 76-82, wherein at least one of said multiphase clocks (MPIC, MPFC) is established by means of a divider (RDIV, FDIV).

84. Asynchrony detector (CD) according to any of the claims 76-83, wherein said at least one output signal (CDO) is established by means of

at least one counter (RCTR, FCTR) and

a digital-to-analog converter (DAC).

85. Asynchrony detector (CD) according to any of the claims 76-84, wherein said at least one output signal (CDO) is established by means of combining the asynchrony detector of claim 82 or 83 with the asynchrony detector of claim 84.

86. Method of establishing an output clock signal (OC) according to any of the claims 1-22, whereby said justification is performed by means of a number-controlled oscillator (NCO) according to claim 59.

87. Method of establishing an output clock signal (OC) according to any of the claims 1-22 or 86, whereby said second block (SBLK) comprises an asynchrony detector (CD) according to any of the claims 76 to 85.

88. Method of establishing an output clock signal (OC) according to any of the claims 1-22 or any of the claims 86-87, whereby said output clock signal (OC) is phase locked to said input timing reference (TR).

89. Method of establishing an output clock signal (OC) according to any of the claims 1-22 or any of the claims 86-88, whereby said output clock signal (OC) is frequency locked to said input timing reference (TR).

90. Method of establishing an output clock signal (OC) according to any of the claims 1-22 or any of the claims 86-89, whereby said output clock signal (OC) is frequency ratio locked to said input timing reference (TR).

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